

FIG.1

(Related Art)

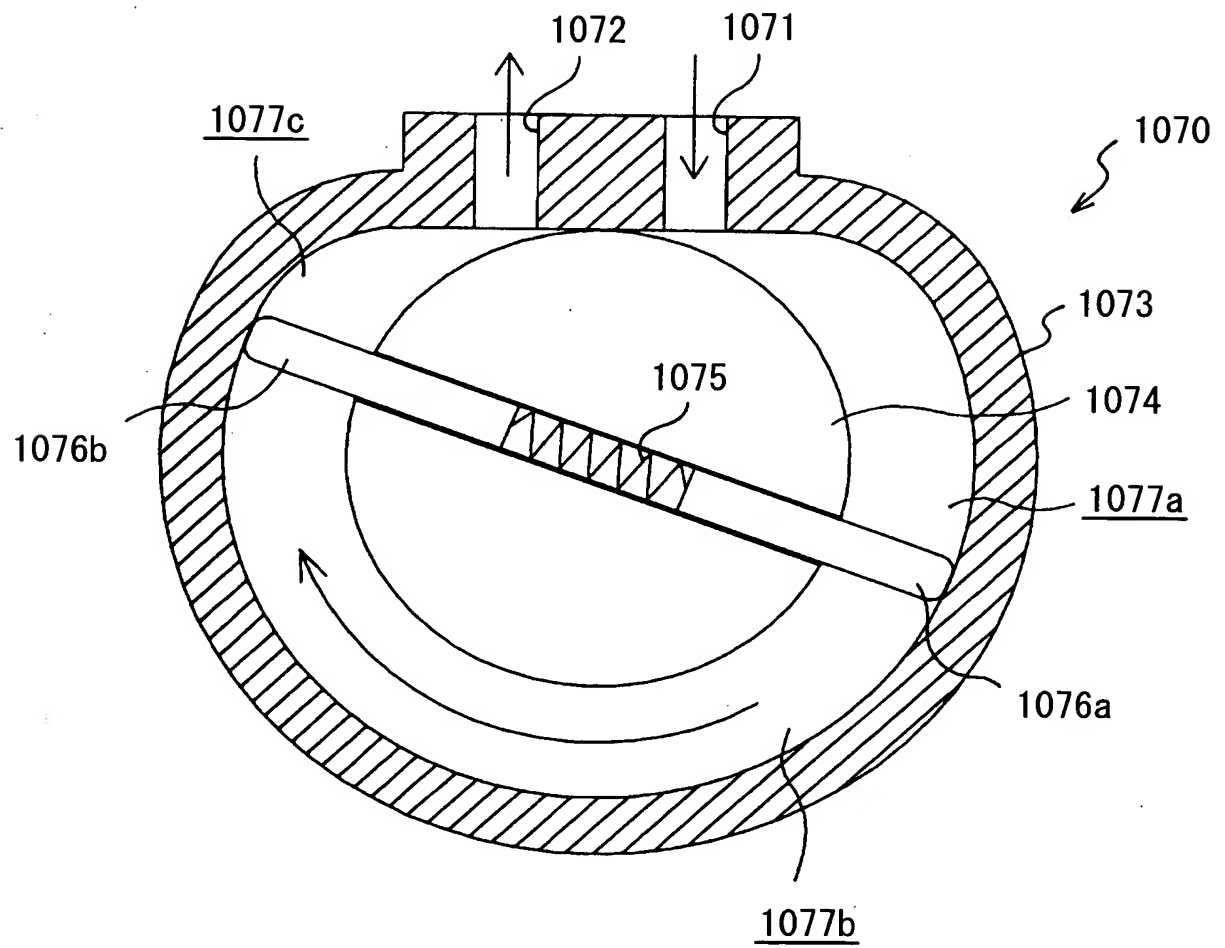


FIG.2

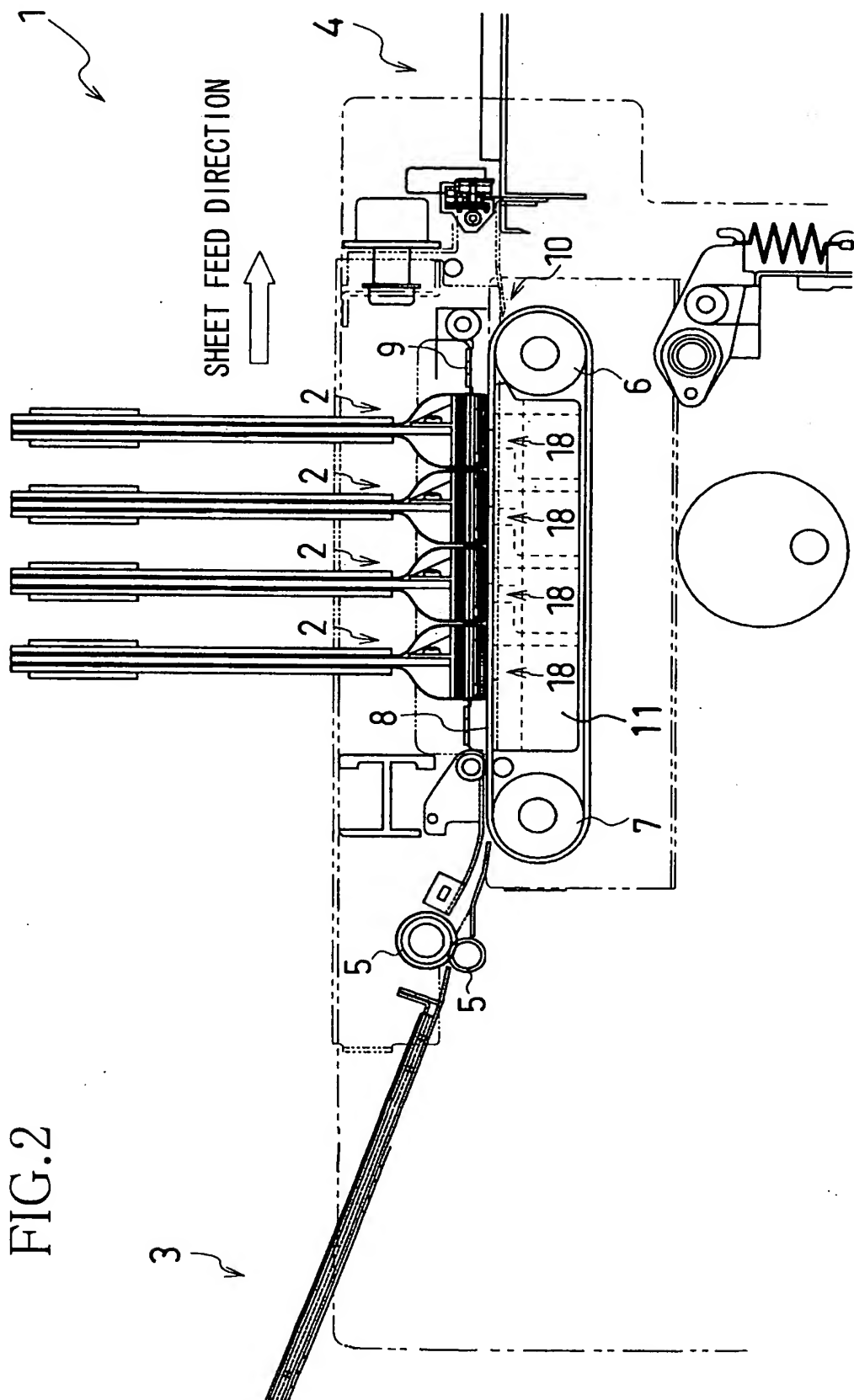


FIG. 3

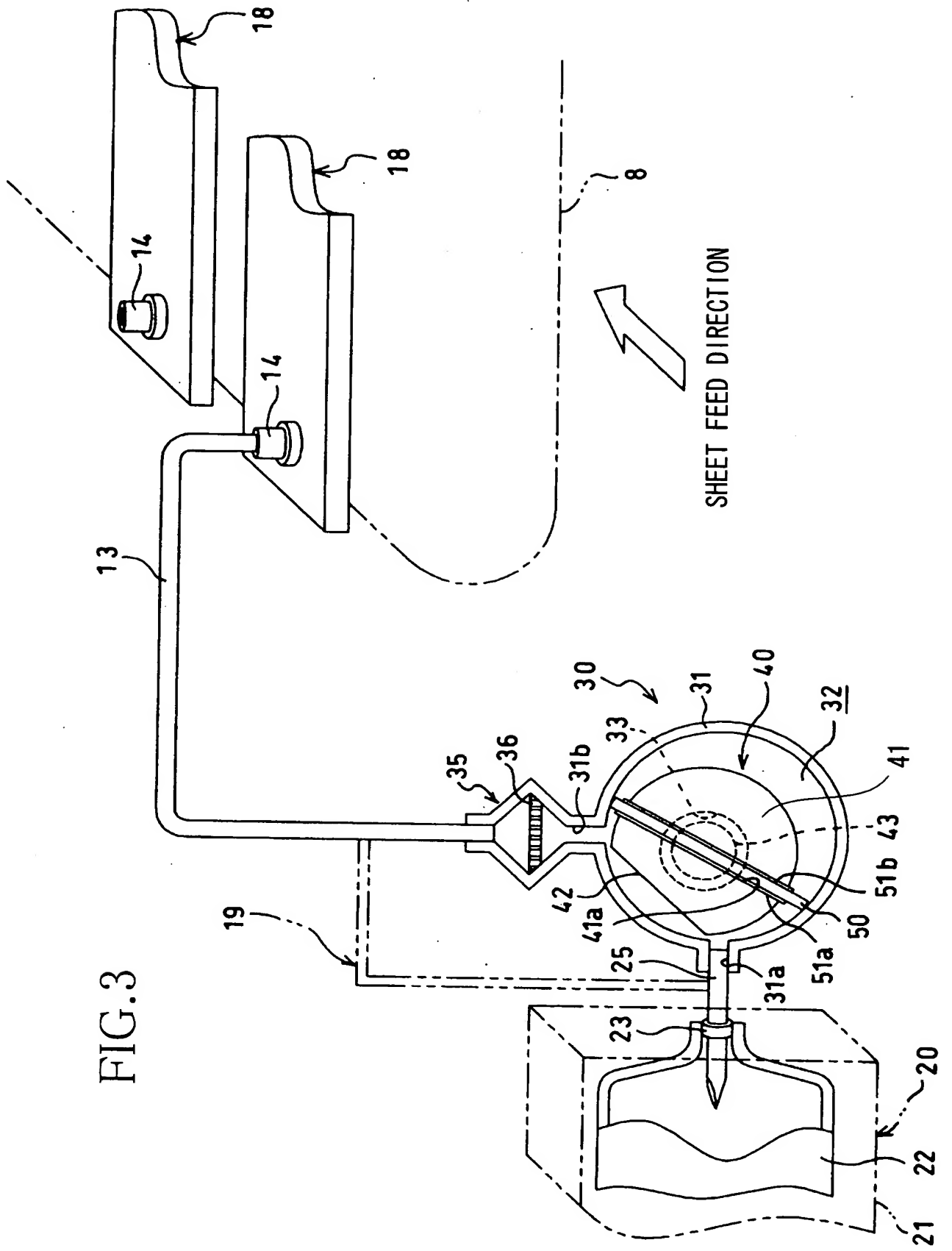


FIG. 4A

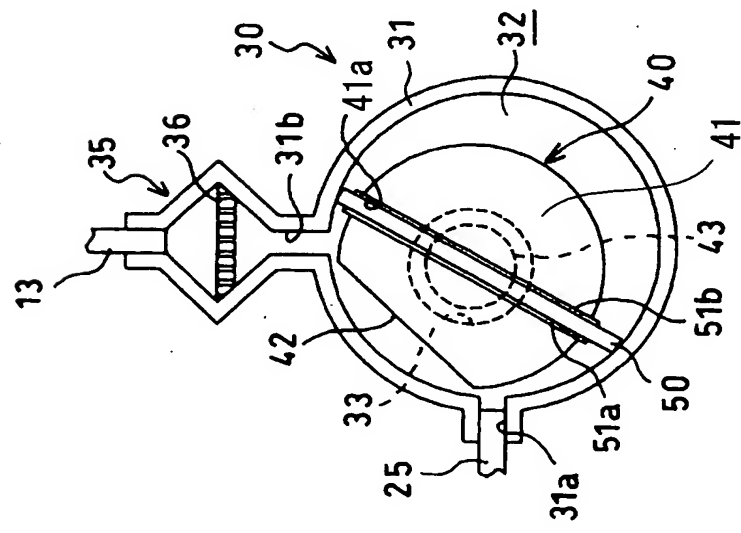


FIG. 4B

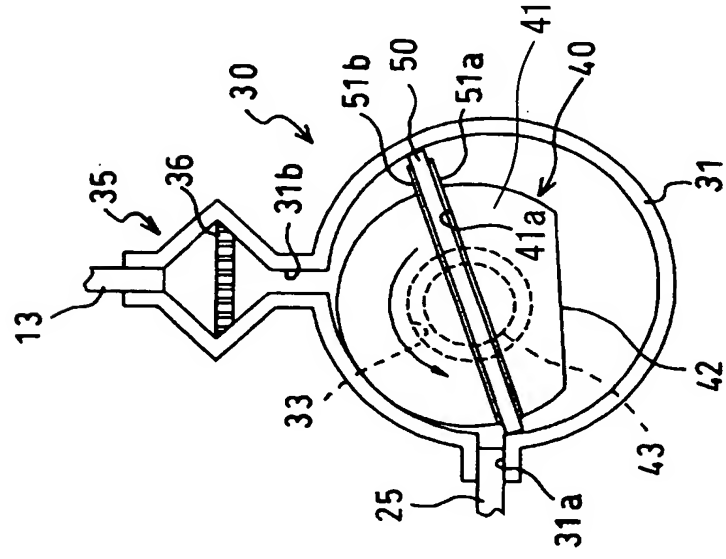


FIG. 4C

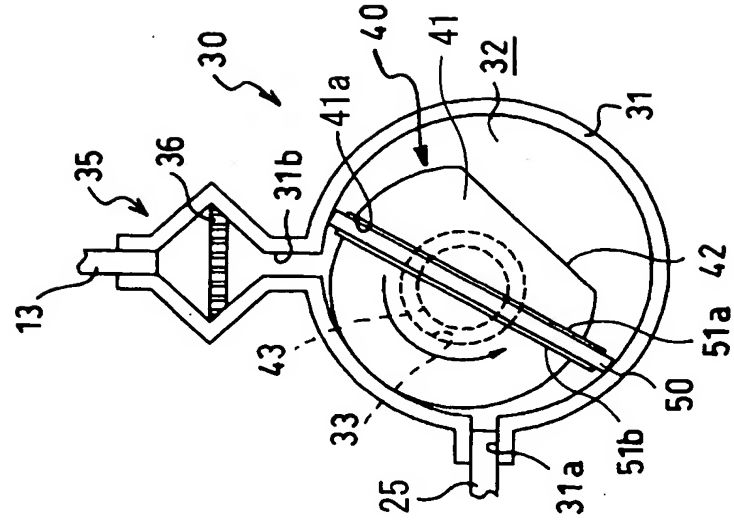


FIG. 5B

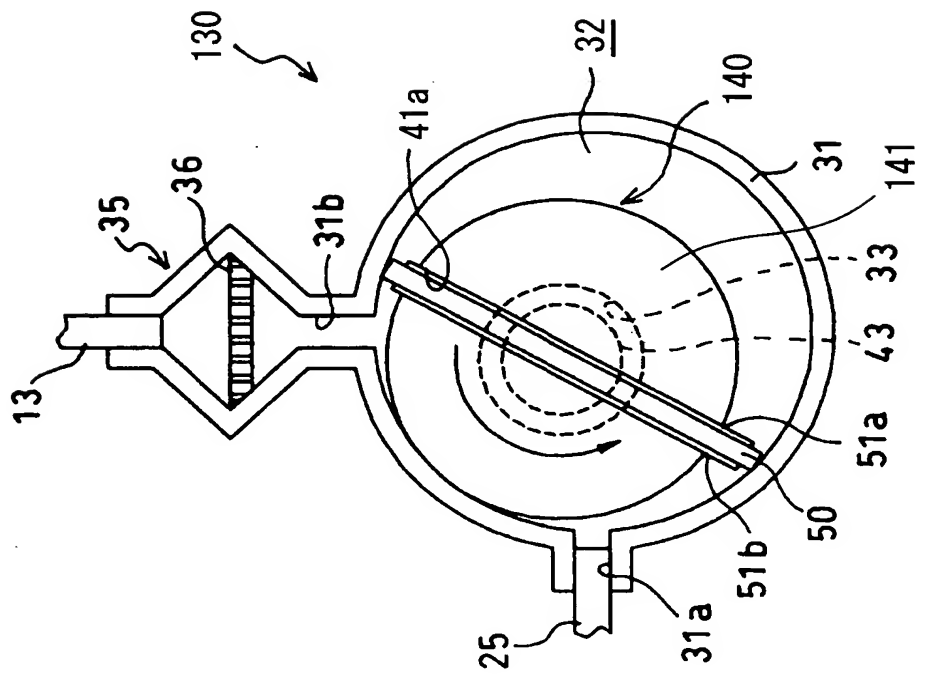


FIG. 6 is a cross-sectional view of a semiconductor device. It shows a central channel region 233 flanked by two gate regions 240 and 249. The gates are formed on a substrate 246. A source/drain region 248 is located under gate 240, and another source/drain region 247 is located under gate 249. A contact layer 245 is shown at the top. Various other layers and features are labeled with reference numerals.

FIG. 7A

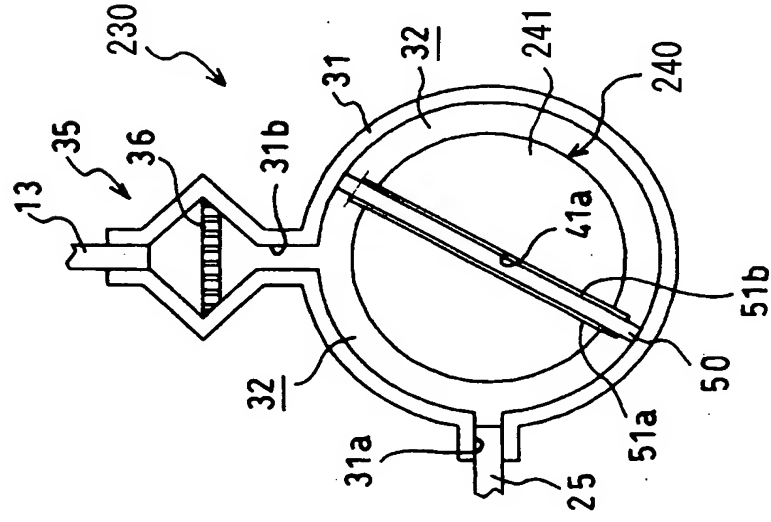


FIG. 7B

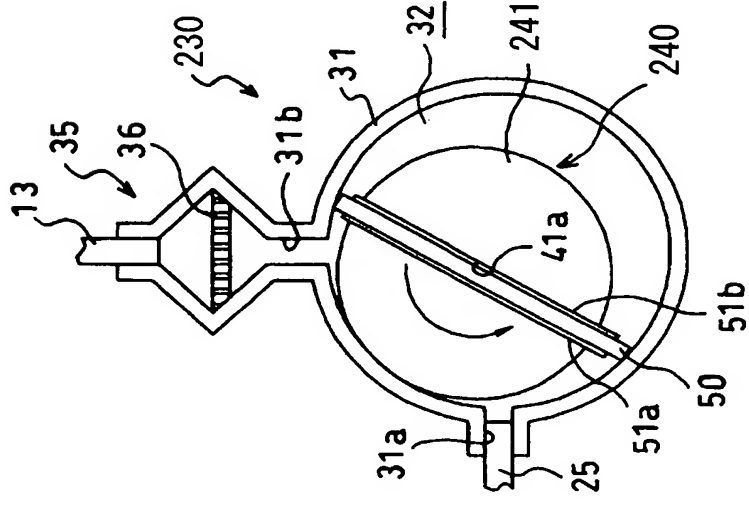


FIG. 7C

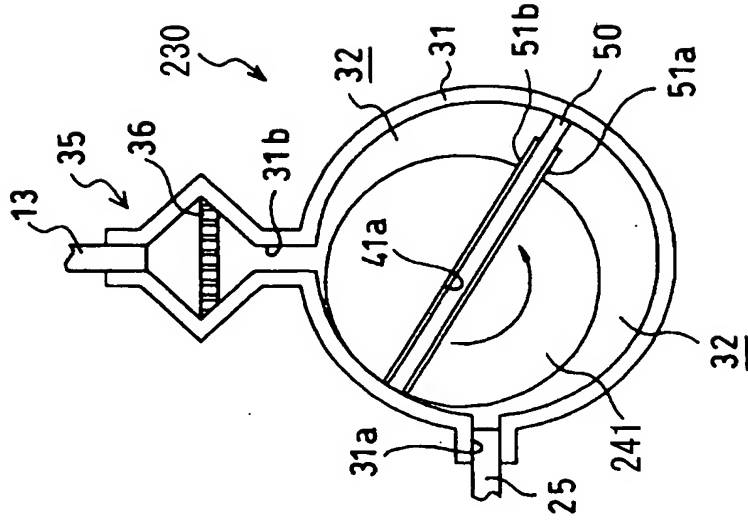


FIG.8A

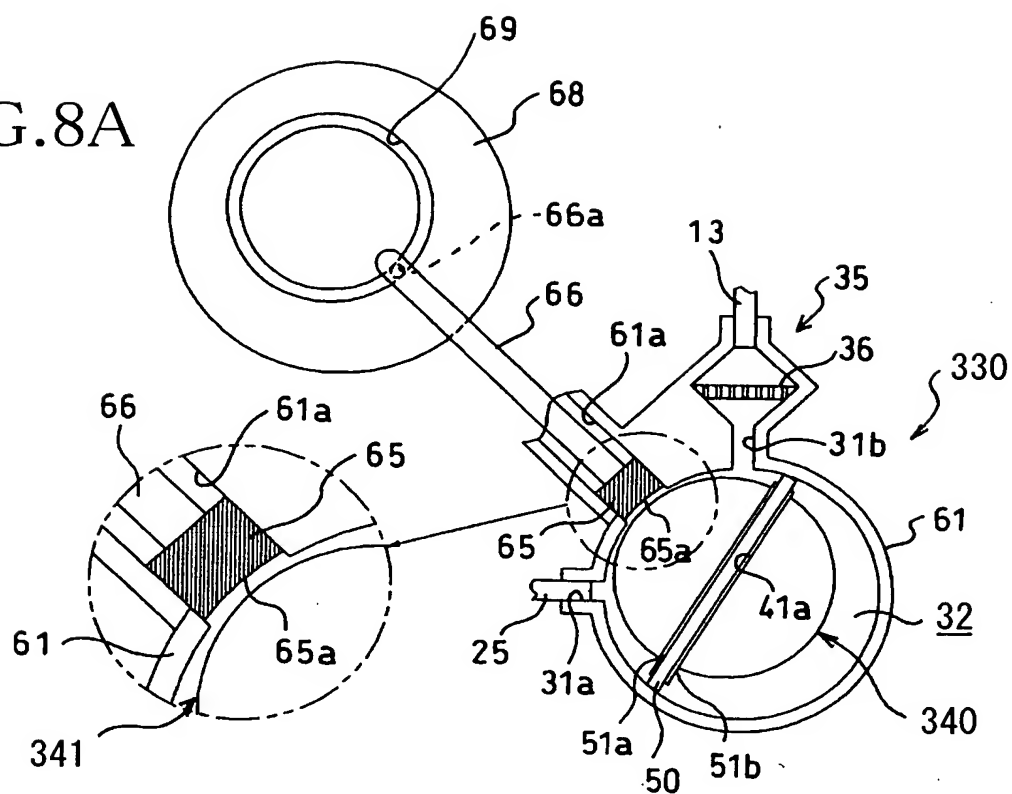


FIG.8B

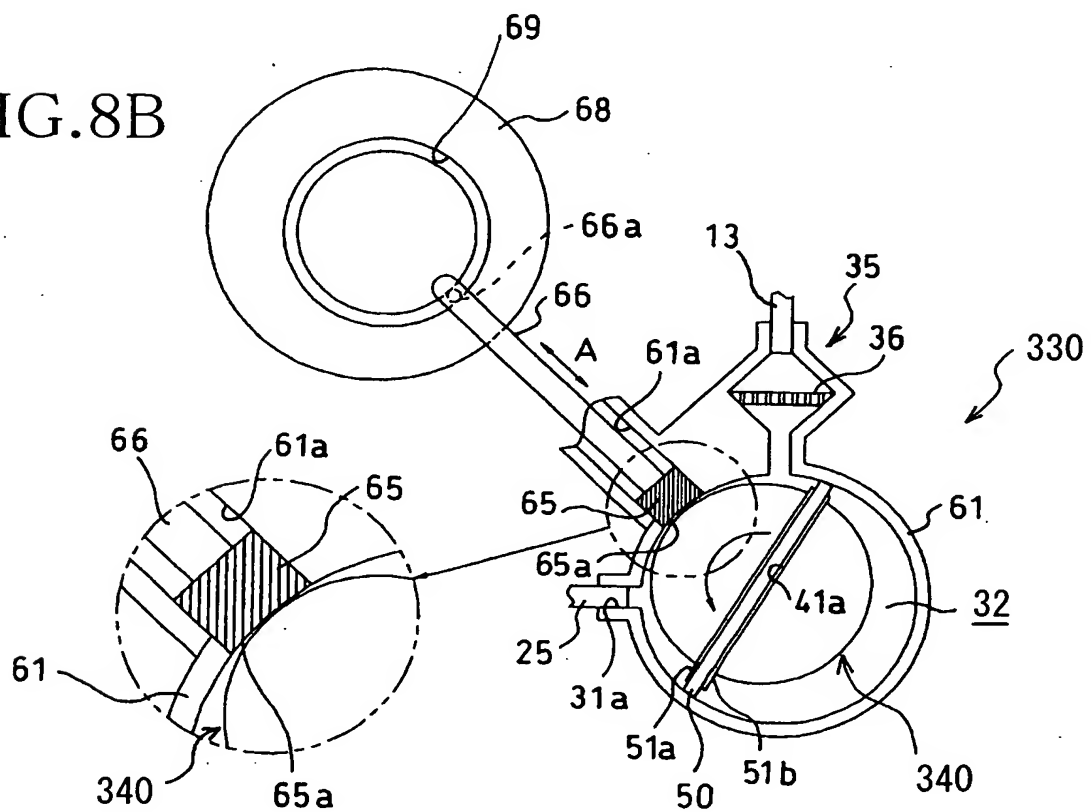




FIG. 9A

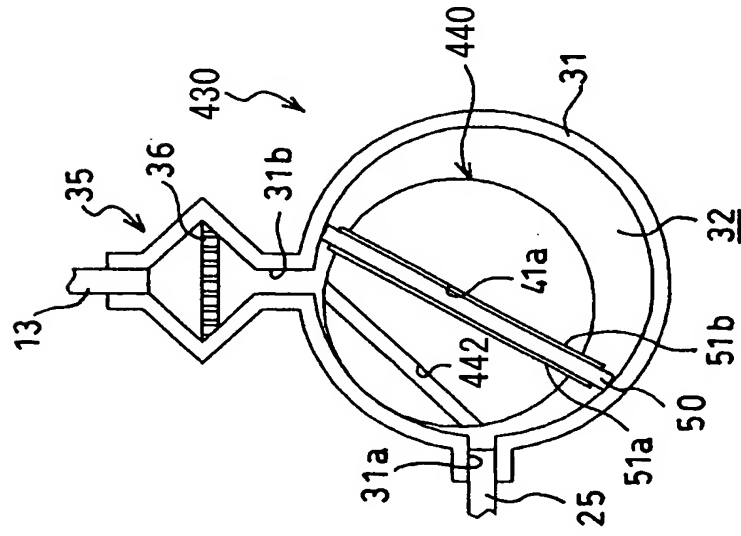


FIG. 9B

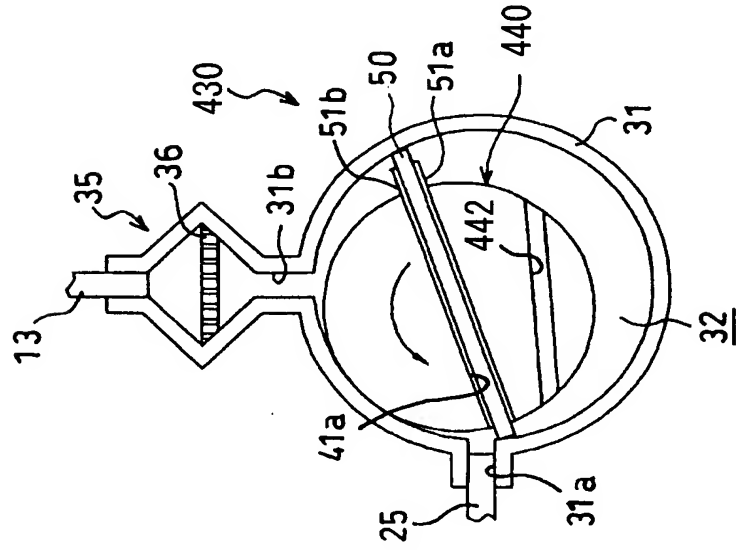


FIG. 9C

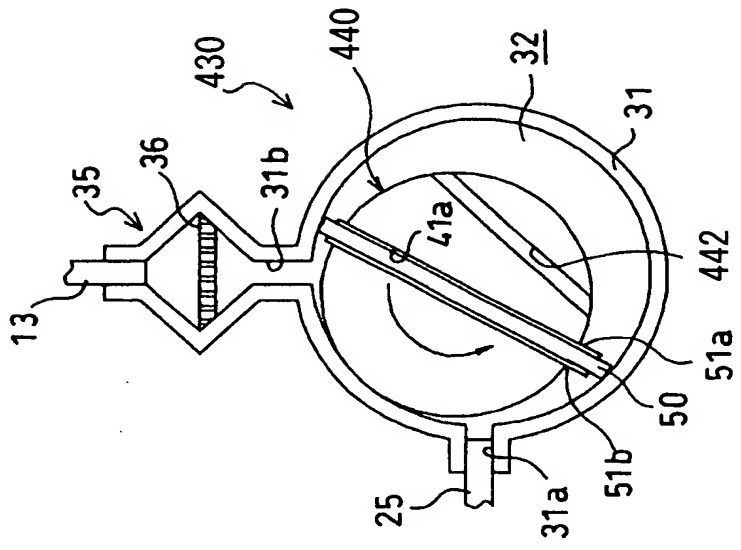
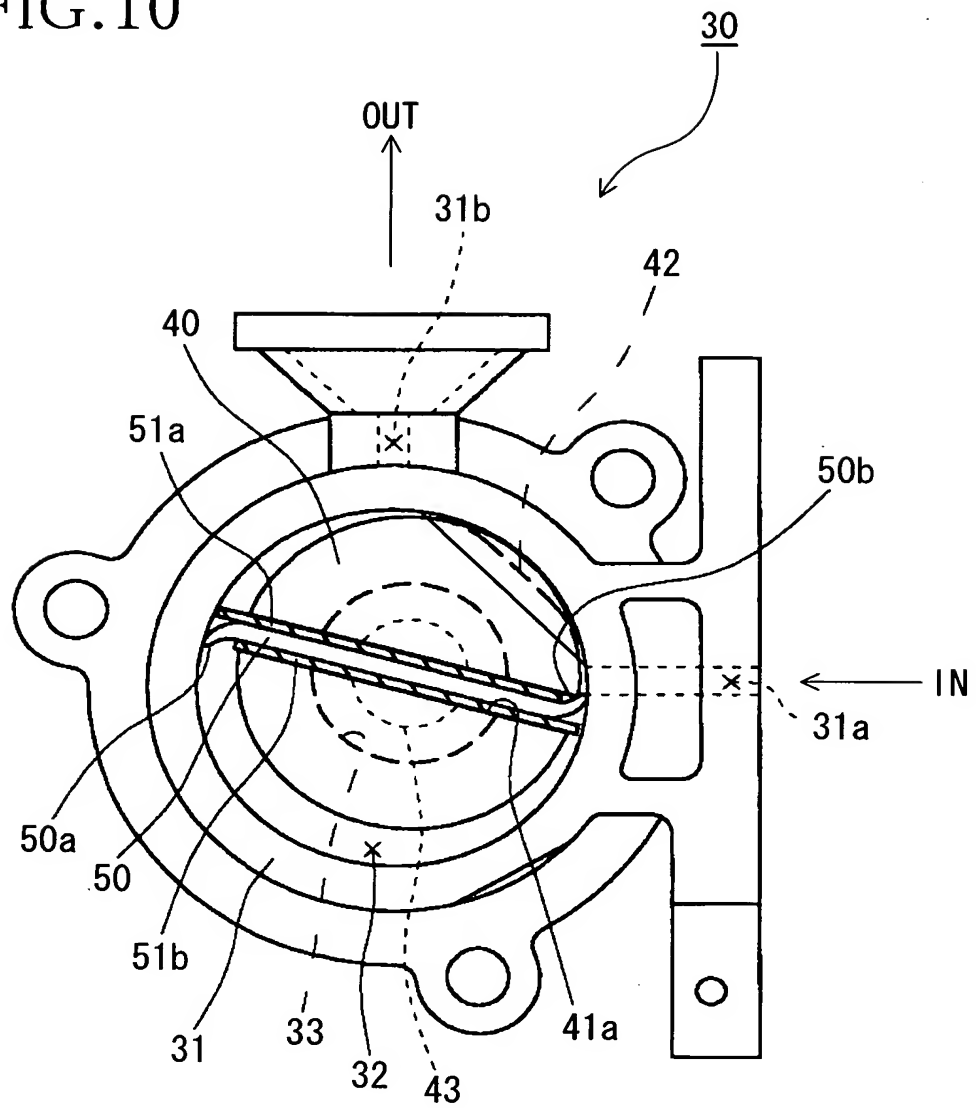


FIG.10



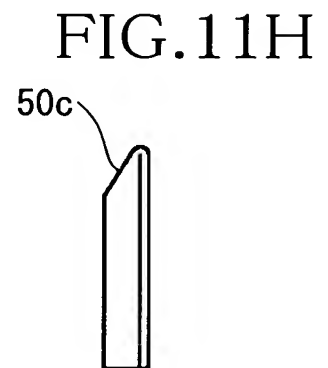
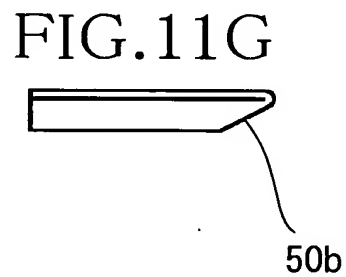
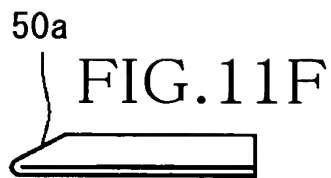
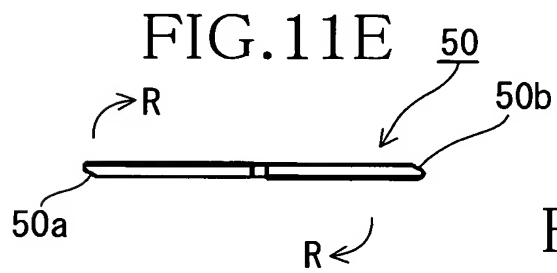
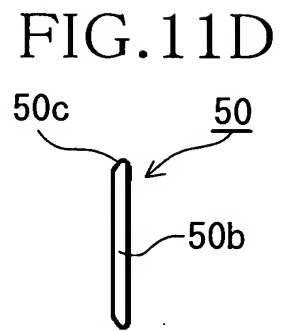
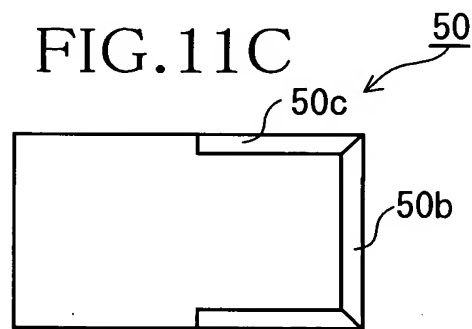
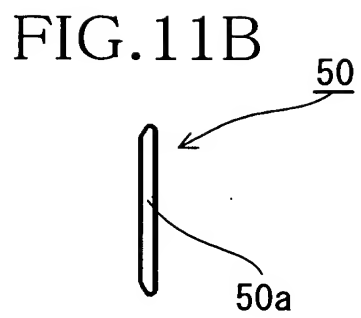


FIG.12A

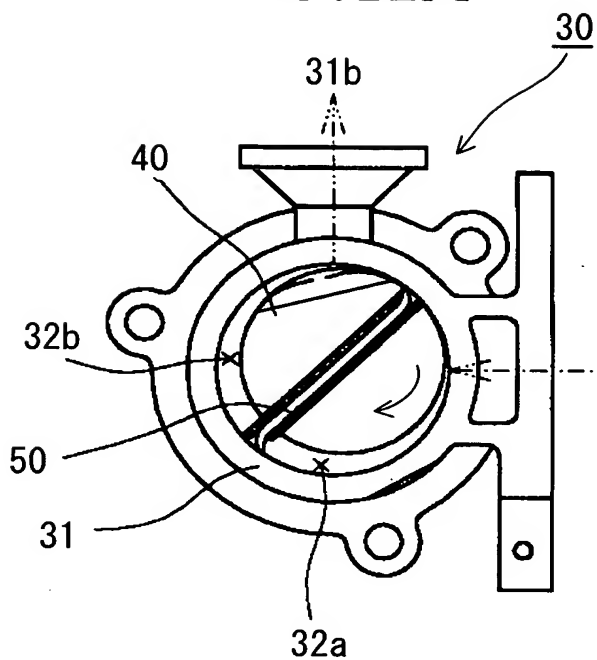


FIG.12C

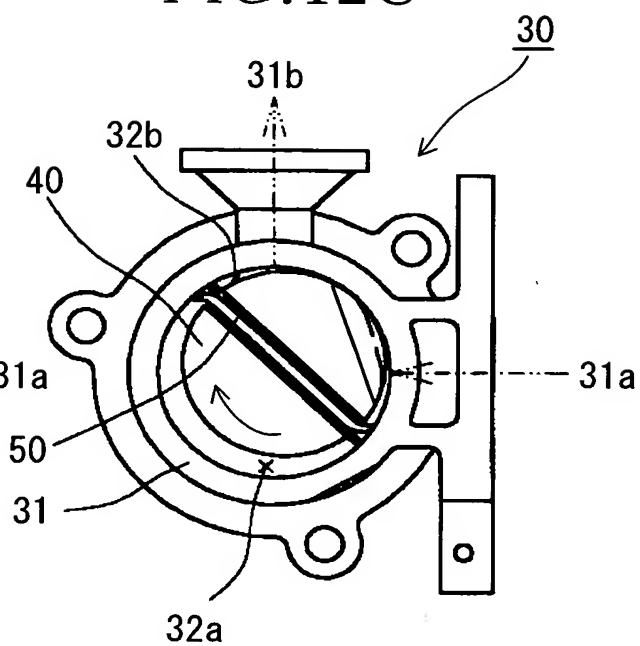


FIG.12B

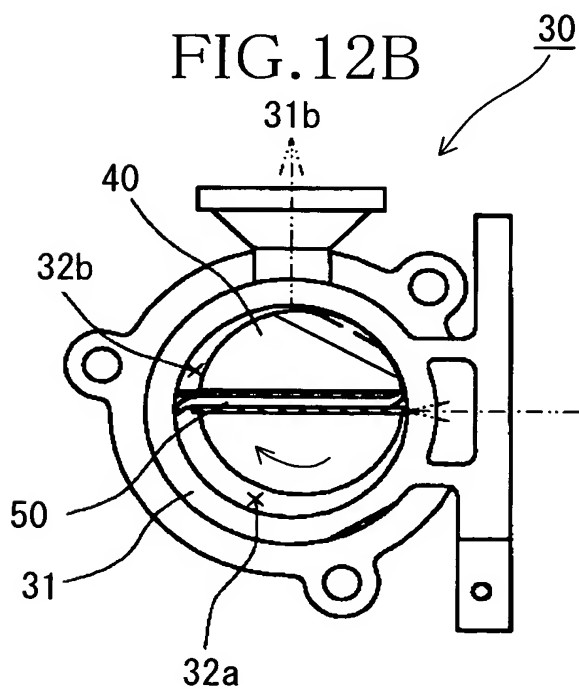


FIG.12D

